Agilent HFCT-5402D 2488 Mb/s Single Mode Fiber Transceiver for SONET OC-48/SDH STM-16 and ATM

Data Sheet

Description

General

The HFCT-5402D is a 1300 nm laser-based duplex SC receptacle 2 x 9 transceiver with integral clock and data recovery circuits. It provides a cost-effective solution for short haul 2488 Mb/s data link requirements.

This compact transceiver requires a single +5 V source and contains the following features as depicted in Figure 1: differential data input, differential retimed data output, differential recovered clock output, laser bias monitor, signal detect and transmitter disable.

Transmitter Section

The transmitter section of the HFCT-5402D is similar to 1300 nm single mode transceivers in use at the 155 and 622 Mb/s rate. It consists of a 1300 nm InGaAsP laser in an eye-safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a custom, silicon bipolar IC which converts differential input PECL logic signal into an analog laser drive current.

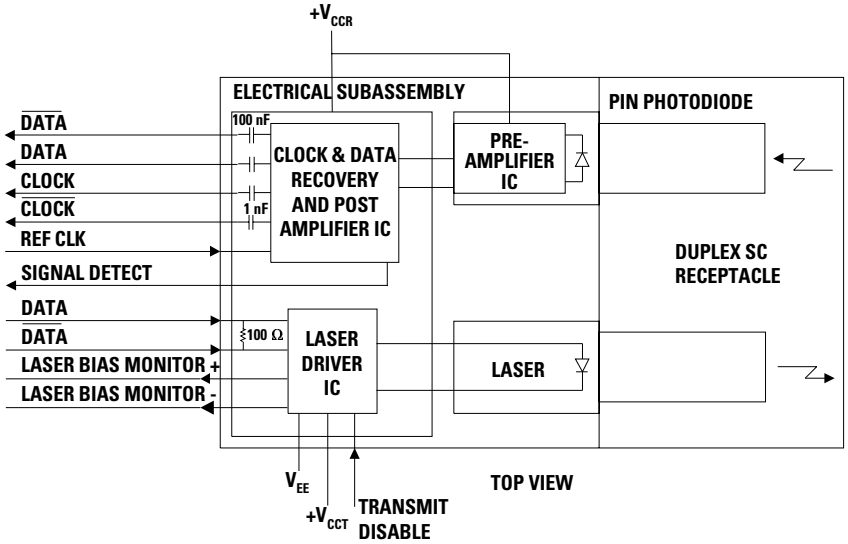

Figure 1. Block Diagram

Features

- 1300 nm single mode transceiver for SONET/SDH short reach links
- Compliant with proposed ATM Forum 2488 Mb/s physical layer specification
- Compliant with SONET jitter tolerance and generation specifications
- Integral duplex SC connector receptacle compliant with TIA/EIA and IEC standards
- Incorporates Agilent's eye safe laser subassembly
- Single +5 V power supply operation
- Integral PLL based clock recovery circuit provides regenerated differential clock and data outputs (CML)
- Transmitter disable function
- Temperature range: 0°C - +70°C
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9001 certified facility

Applications

- ATM 2488 Mb/s links
- SONET OC-48/SDH STM-16 interconnections

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Receiver Section

The receiver section of the transceiver provides a full set of features including an integral clock and data recovery (CDR) circuit together with signal detect function.

The receiver utilizes an InGaAs PIN photodiode mounted together with a transimpedance preamplifier IC. This is connected to custom silicon circuits providing post-amplification and quantization, CDR function and signal detection.

CDR Function

In normal operation, the CDR data loop is able to acquire and maintain bit lock with the use of the external reference clock. The recovered clock is used to re-time the quantizer data output, which completes the full CDR function.

The relative timing relationship between the output retimed data and the recovered clock signals is shown graphically in Figure 2. The voltage swing measurement method is also shown for clock and data outputs.

For input optical power greater than the specified receiver sensitivity of -18.5 dBm, the bit-error-ratio will be better than 1×10^{-10}. The SD (signal detect) will be deasserted when loss of optical signal occurs.

Reference Clock

With 'intermittent' or 'no data condition' the output clock will slowly drift away from the 2.48832 GHz. The reference clock enables the VCXO to acquire and maintain lock. Ref Clk input is self biasing and 50 Ω input terminated.

Temperature Range

The HFCT-5402D is specified for operation over normal commercial temperature range of 0° to +70°C with recommended metal shield in place (see Figure 3) and with 2 m/s forced airflow around the transceiver. In the event a 2 m/s airflow is not available due to chassis restrictions, high temperature operation will be limited to +60°C.

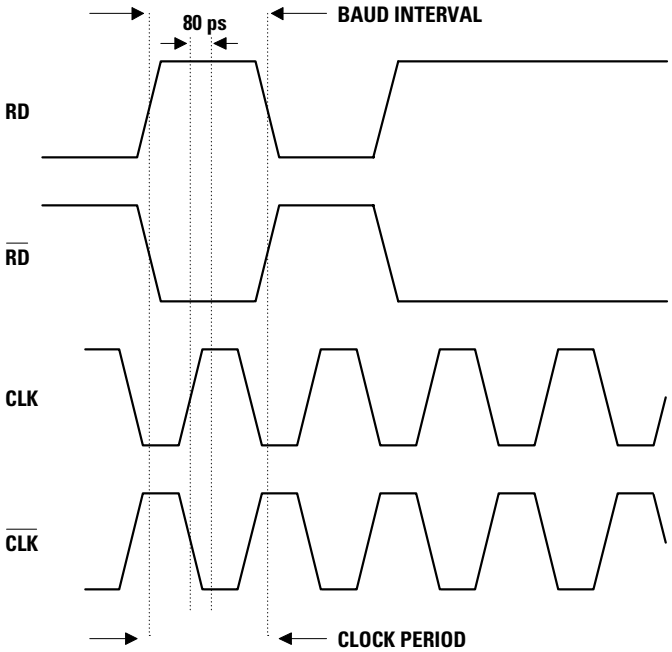


Figure 2a. Relative Timing Relationship Between Output Retimed Data and Recovered Clock Signals

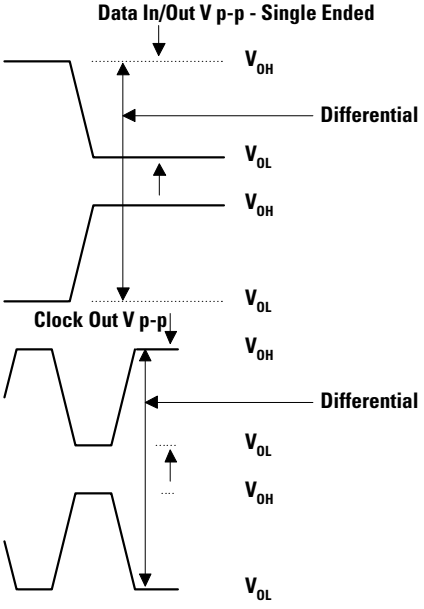


Figure 2b. Logic Voltage Values

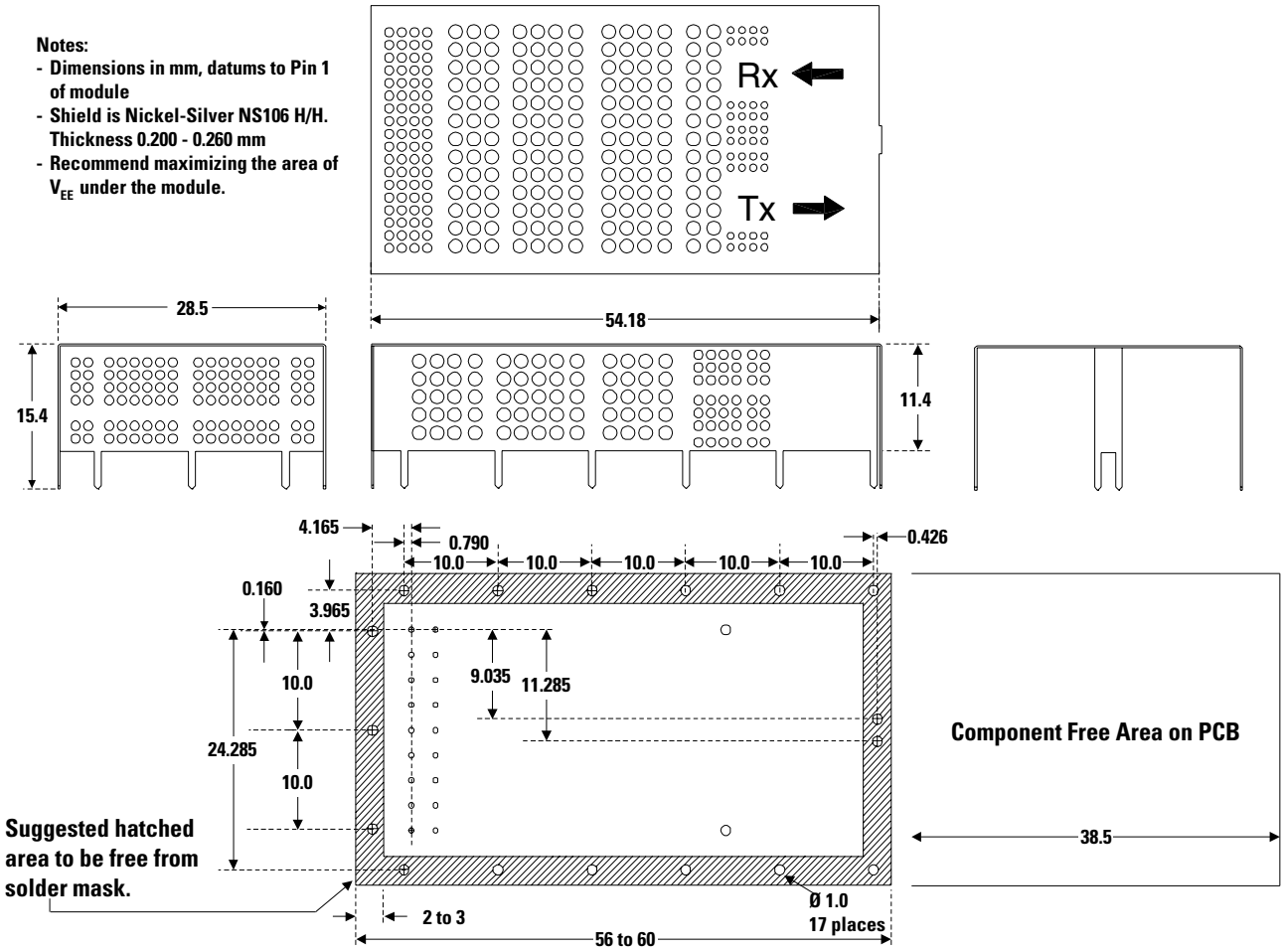


Figure 3. EMC Diffuser Shield for HFCT-5402D Transceiver (Mounted Inboard)

Application Information

Transmitter Section

The HFCT-5402D transmitter section comprises Agilent's proprietary high speed silicon bipolar laser driver IC and Multi-Quantum Well (MQW) laser diode housed in an eye-safe optical subassembly. The input stage accepts PECL level signals and converts this to analog laser drive current. The laser driver IC provides both laser bias and modulation current control enabling a physically compact transmitter section. The nonlinear characteristics of laser threshold and bias points over operating temperature range utilizes sophisticated extinction ratio control circuitry. The Agilent laser driver IC deploys a tri-gradient approximation methodology and allows good power and extinction ratio control. Figure 4 illustrates the sections of the laser driver IC.

Electrical Characteristics
Transmitter Section
Input Stage

The input stage is internally biased and 50 ohm terminated. The transmitter accepts either single-ended or differential PECL inputs with signal levels ranging from 200 mV to 1100 mV swing. It is important to ensure data input lines have a 50 ohm characteristic impedance for optimum performance.

Laser Bias Monitor

The laser bias monitor points (pins 5 and 6) allow the user to directly measure dc bias current (see Figure 5). The I/V relationship for laser bias current is:

$$I_{BIAS} = [(V_6 - V_5)/10] \text{ A}$$

It is worth noting that the above relationship yields total laser forward current (threshold and bias) when no data is applied and approximately threshold current when modulation is applied. This monitoring facility allows the user to identify EOL conditions in a given application.

Figure 6 shows a circuit which can be used for indicating high bias current conditions. Pins 5 and 6 are connected to the inverting and non-inverting inputs of IC1A respectively. IC1A is configured as a unity gain buffer and its output (V_{IC1A}) fed to IC1B. IC2 provides a fixed 1.25 V reference to VR1 which allows fine adjustment for setting the threshold voltage (V_{TH}) at IC1B which is configured as a TTL comparator. The voltage V_{TH} at IC1B's inverting input determines the level at which the high bias conditions results in a TTL flag. For End of Life indication, a typical voltage setting for V_{TH} is:

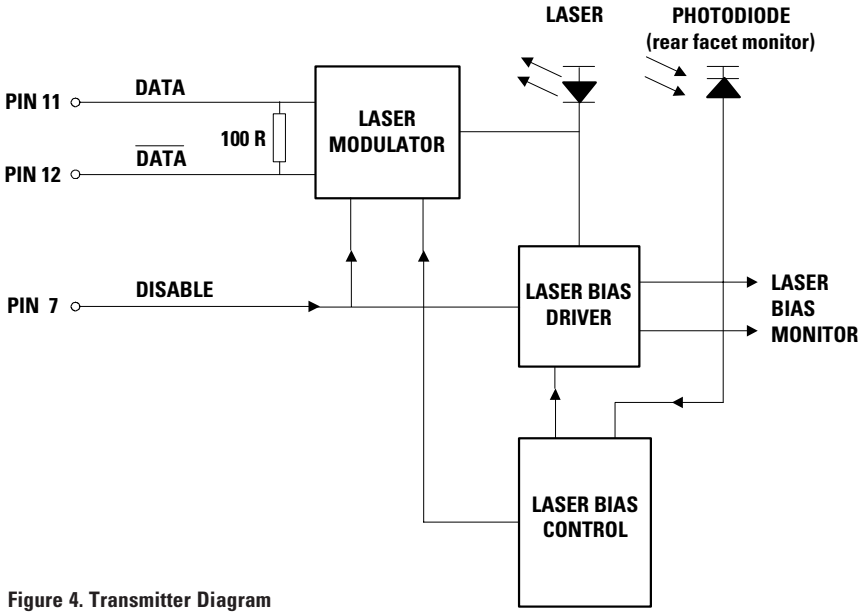


Figure 4. Transmitter Diagram

3*(V_{IC1A} at +25°C, no input data modulation) for operation between +25°C - +70°C

1.5*(V_{IC1A} at +25°C, no input data modulation) for operation between 0 - +25°C

These ratios are approximate and represent a coarse EOL indicator when used in conjunction with the circuit shown.

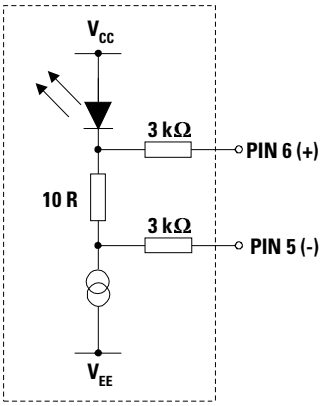


Figure 5. Bias Monitor

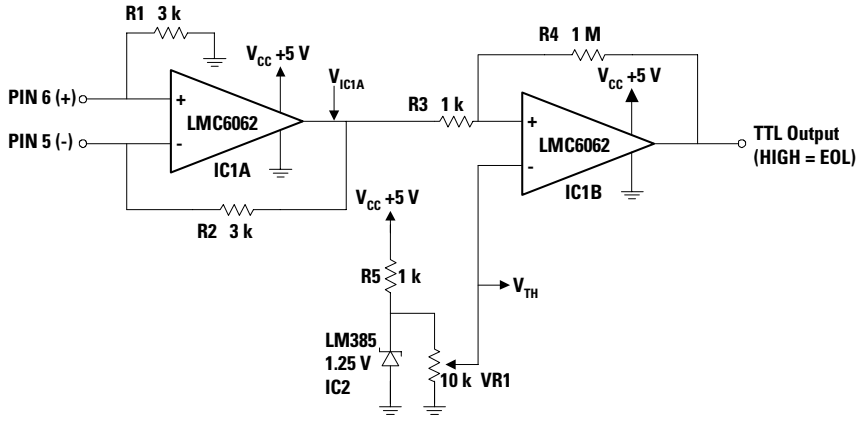


Figure 6. Laser Bias Indicator Circuit

Transmitter Disable

The transmitter can be disabled by connecting pin 7 to the appropriate voltage (V7 ≥ 4 V). In normal operation (transmitter enabled), no external connection is required.

Transmitter Jitter Generation

The jitter generation requirements for SONET/SDH transport systems are:

- 100 m UI pk - pk (SONET)
- 10 m UI rms (SONET/SDH)

Typical jitter generation performance for the HFCT-5402D is:

- 60 m UI pk - pk
- 6 m UI rms.

Figure 7 shows the experimental configuration used to test jitter generation.

An Agilent 70841B pattern generator is used to generate ECL data at 2.48832 Gb/s to modulate the transmitter. Jitter generation is measured using a SONET STS48 2^{23} PRBS scrambled pattern.

The optical output of the transmitter is attenuated and fed into the receiver of the OmniBER 718A at an input sensitivity of -14 dBm.

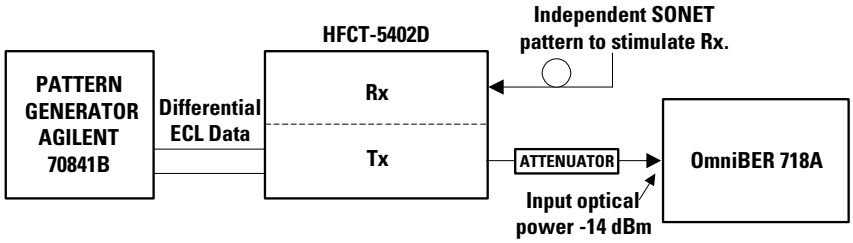


Figure 7. Jitter Generation Test Configuration.

Receiver Section
Reference Clock

The clock and data regeneration function is designed such that a reference clock running at 1/128th the data rate is required to acquire and maintain lock. Operation at other clock frequencies in the vicinity of 2.488 GHz are possible by using different crystal oscillators having 1/128th the frequency of interest. (for 2488 Mb/s operation a 19.44 MHz clock is required). Figure 8 illustrates the receiver operation.

Inputs fed to the reference clock (pin 1) require 100 nF ac coupling and need 100 ppm frequency accuracy. Clock outputs are maintained at 2.48832 GHz throughout the dynamic range of the receiver up to the threshold of Signal Detect. In the absence of input optical data, the transceiver clock will vary within 1000 ppm of the clock frequency.

All development and characterization work have been performed with a PECL 19.44 MHz clock oscillator part number OSO-SFE-B00C obtained from Onspec (www.onspec.co.uk). Figure 9 shows the rise time and amplitude requirements for the reference clock input. Various combinations of rise times and amplitudes allow the user a degree of freedom in selecting clock sources.

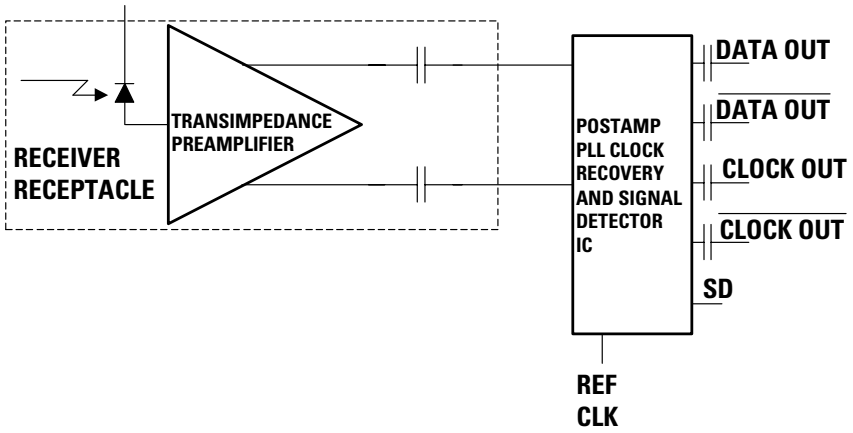


Figure 8. Receiver Block Diagram

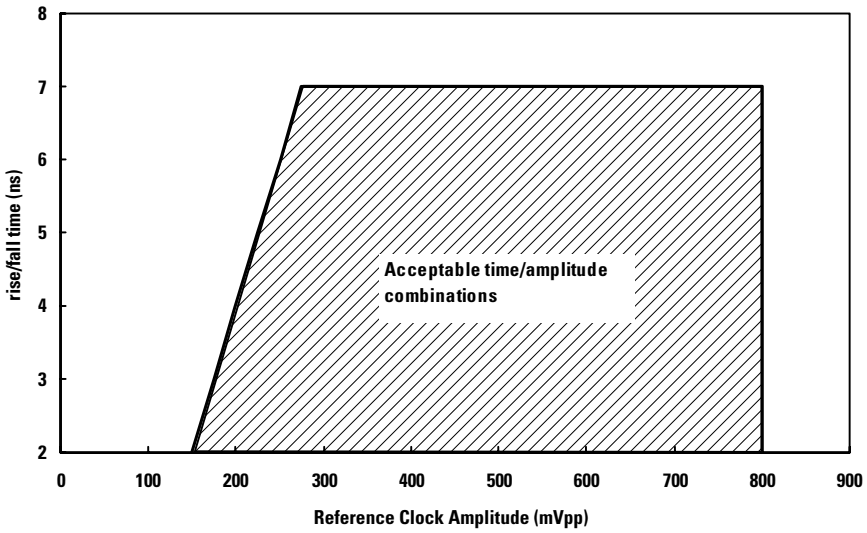


Figure 9. Reference Clock Rise and Fall Times Versus Amplitude

Output Terminations

The receiver DATA and CLOCK outputs provide Current Mode Logic (CML) levels. These outputs are internally ac coupled with 0.1 uF capacitors. Typical output swings are in the order of 350 mV for DATA and 300 mV for CLOCK. Figures 10 and 11 show typical data and clock waveforms.

It is recommended that the receiver outputs are connected to 50 ohm transmission lines. Interfacing with ECL/PECL input stages is possible provided that input sensitivities will accommodate minimum voltage swings of 200 mV pk-pk.

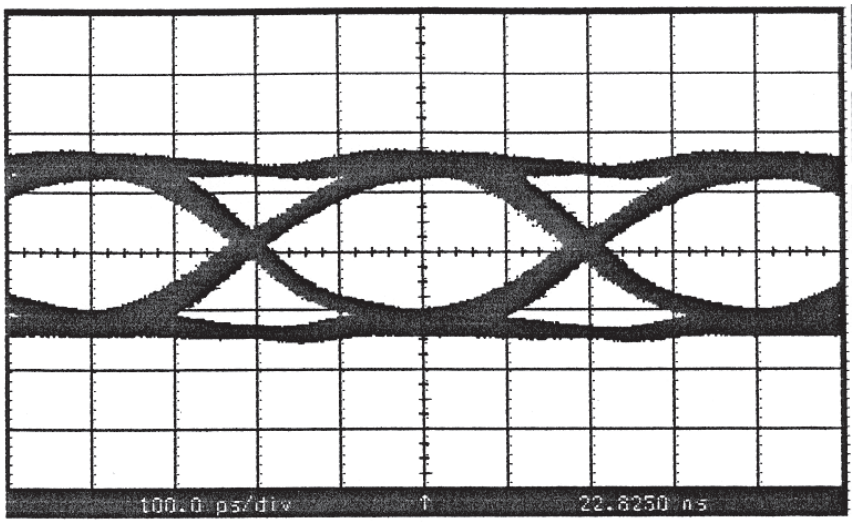


Figure 10. Typical Receiver DATA Output 2488 Mb/s.

Signal Detect

The signal detect function is provided via a single-ended output and offers low power TTL capability. Interfacing this node to other stages requires a high impedance input typically in the order of 10 K ohms. Low input impedance stages are unsuitable. This node may be left unconnected if not used. Hysteresis for the signal detect function is typically 0.1 dB.

Figure 12 shows a circuit that is recommended for interfacing the +5 V TTL SD output into a +3.3 V LVPECL input. The SD node comprises a PNP transistor with a collector resistance of 4.7 K.

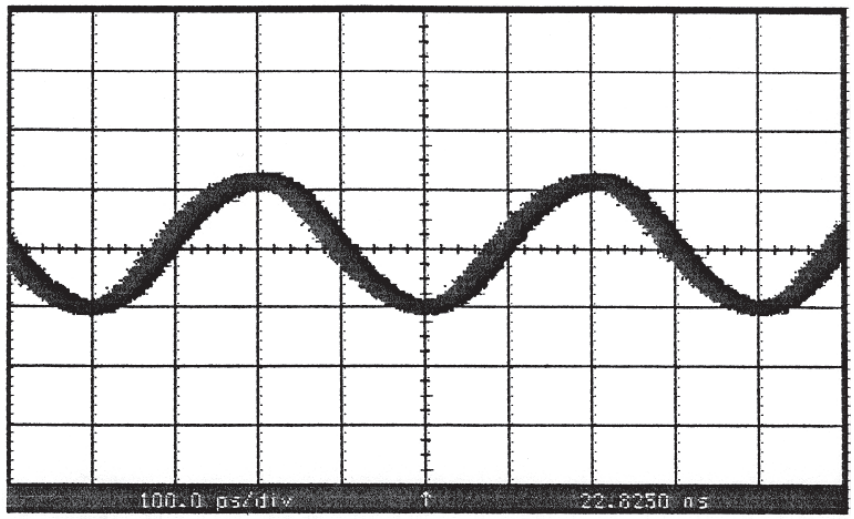


Figure 11. Typical Receiver CLOCK Output 2488 MHz.

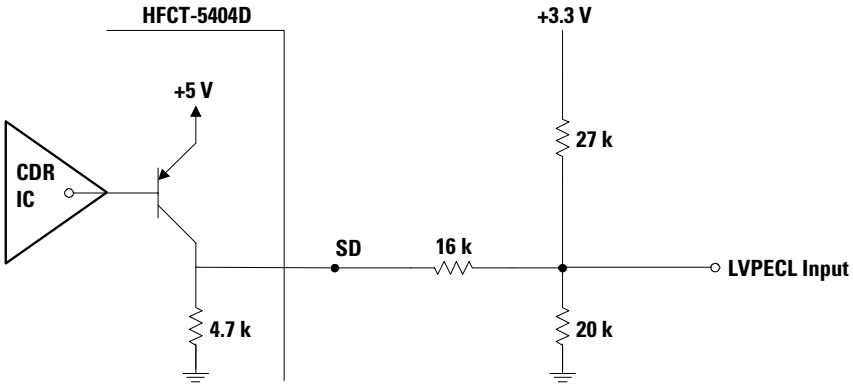


Figure 12.

Jitter Parameters

The HFCT-5402D transceiver design fulfills the jitter generation and tolerance requirements for SONET and SDH. Figure 13 shows typical jitter tolerance performance. Jitter transfer performance does not conform to SONET/SDH requirements due to a slightly higher cutoff frequency. However, in-band jitter transfer performance has no peaking. Typical jitter transfer performance is shown on Figure 14.

Reflectance

It is recommended that an 8° angle polished SC connector be used in conjunction with the HFCT-5402 in order to fulfill the reflectance requirements as per ITU-G957 and Bellcore GR-253-CORE. Optical reflection on the Rx side of the transceiver is primarily contributed by the glass air interface of the SC connector ferrule. An angle polished connector for such an interface reduces the incidental refection.

Receiver Operating Wavelength

The HFCT-5402D receiver is specified for operation over a range of wavelengths from 1270 nm to 1570 nm. Figure 15 shows the typical dc responsivity curve of an InGasAs PIN Photodiode.

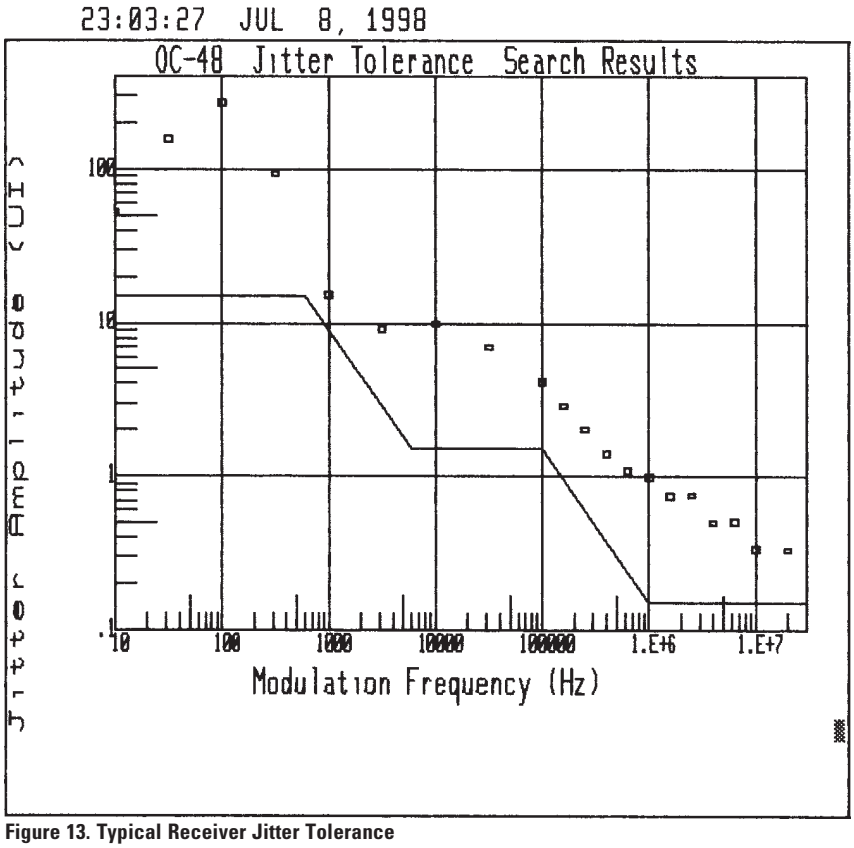


Figure 13. Typical Receiver Jitter Tolerance

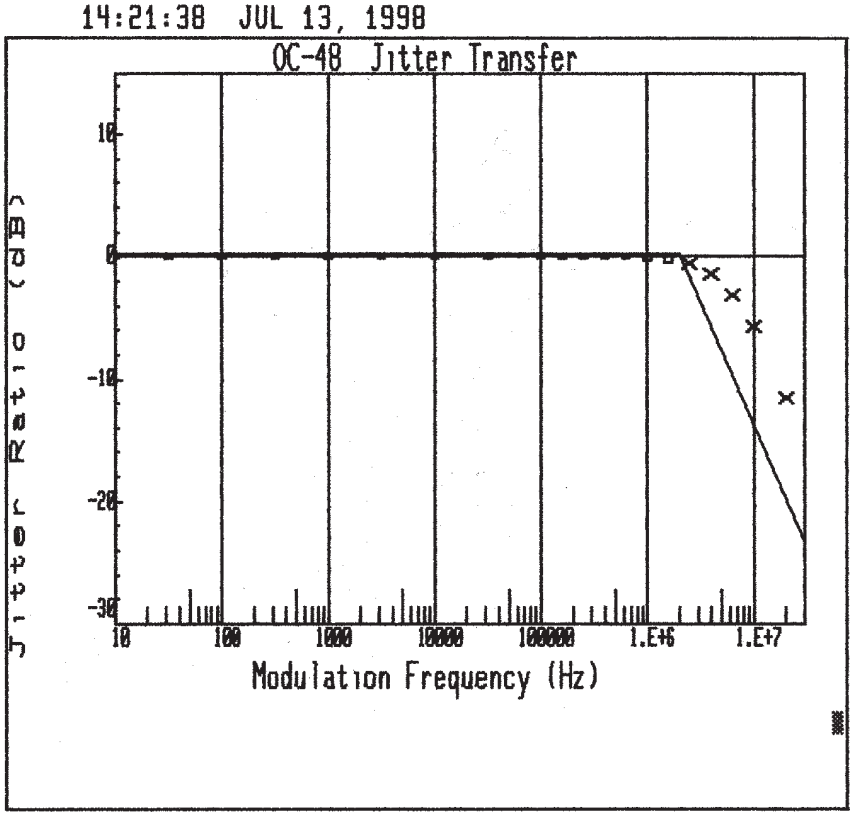


Figure 14. Typical Receiver Jitter Transfer

Power Supply Filtering

Good power supply filtering is required for optimum receiver performance. The LC filtering technique illustrated in Figure 16 is recommended for the user. This configuration of filtering arrangement is adopted for the HFCT-5402D evaluation board. Figure 17 shows the noise rejection response for such an configuration. Additional information is provided in Figure 18 to show noise rejection when the series inductor value is increased to 47 uH. Using an intermediate value of series inductance allows the designer to balance physical size, ohmic resistance (and hence voltage drop) and filtering capability to suit application needs.

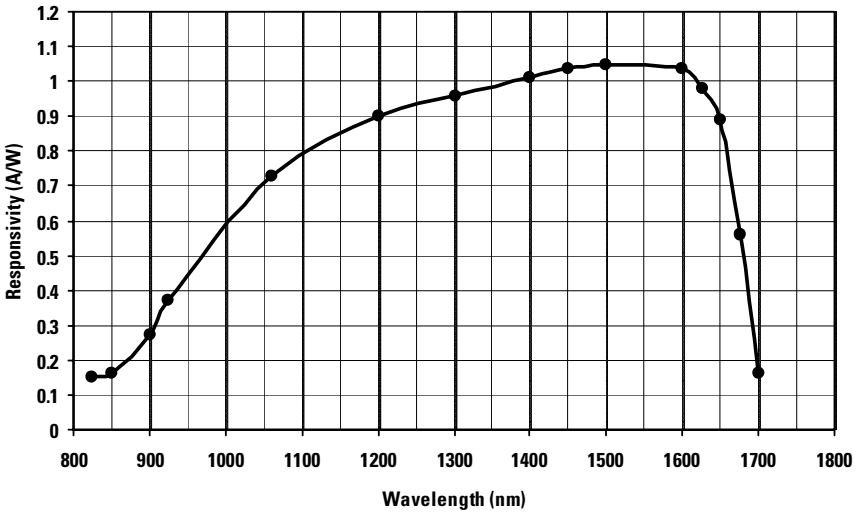


Figure 15. Typical dc Responsivity of an InGasAs PIN Photodiode

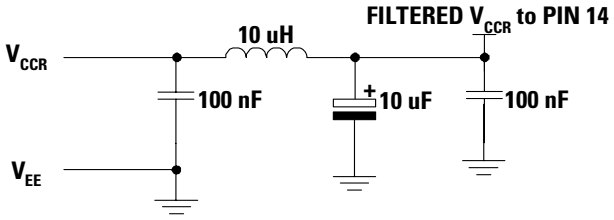


Figure 16. Filter Network for Power Supply Noise Reduction

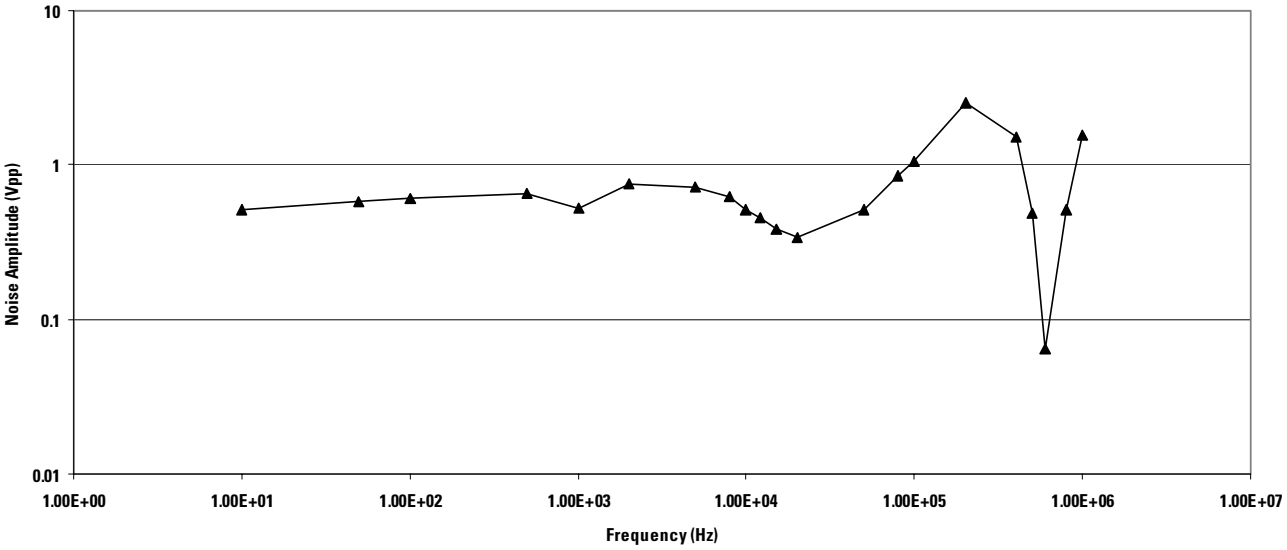


Figure 17. Power Supply Noise Rejection with 10 uH Inductor(-1 dB Receiver Sensitivity)

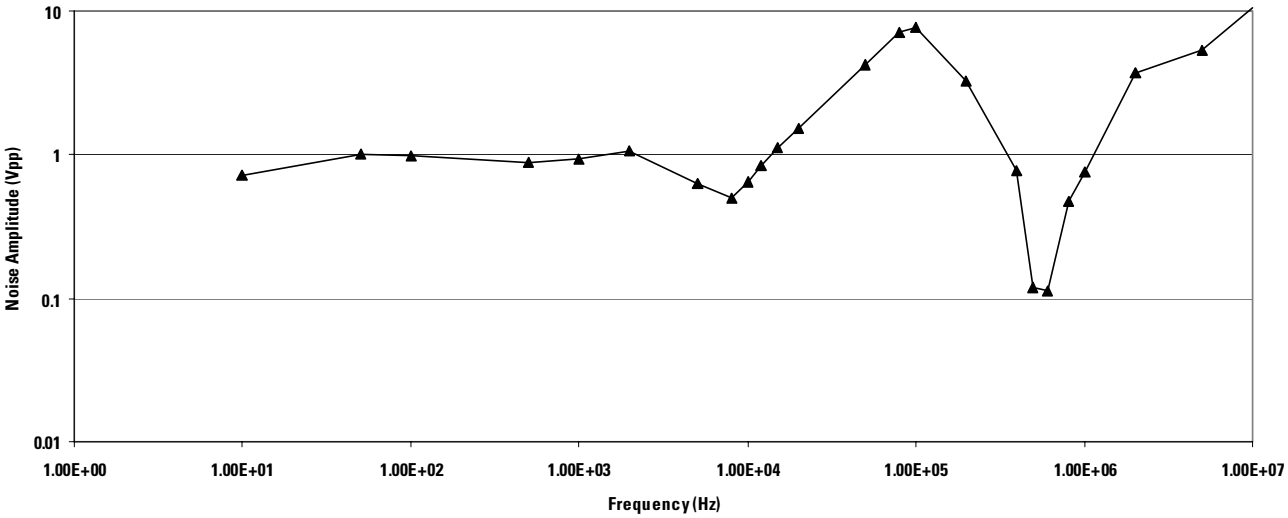


Figure 18. Power Supply Noise Rejection with 47 uH Inductor (-1 dB Receiver Sensitivity)

Evaluation Board

An evaluation board (HFCT-5001) is available for easy use and demonstration of transceiver performance. The evaluation board is shown in Figure 19 and provides a physical platform for the device under test and offers facilities for +5 V dc power supply connections, Tx data inputs, signal detect, Rx data/clock outputs, clock reference input, Tx disable switch and recommended power supply filtering.

The evaluation board also provides a 19.44 MHz crystal oscillator which is powered by the +5 V dc voltage supply. The output of this unit is connected to the clock reference input of the first transceiver and allows the HFCT-5402D to operate at 2.488 Gb/s data rate. Optionally, a separate clock source can be fed to the first board if a different frequency is required.

It is possible to operate the HFCT-5402D between 622 Mb/s to 2.66 Gb/s. However, full performance characterization has only been performed at 2.488 Gb/s line rate.

The circuit schematic for the evaluation board is shown in Figure 20.

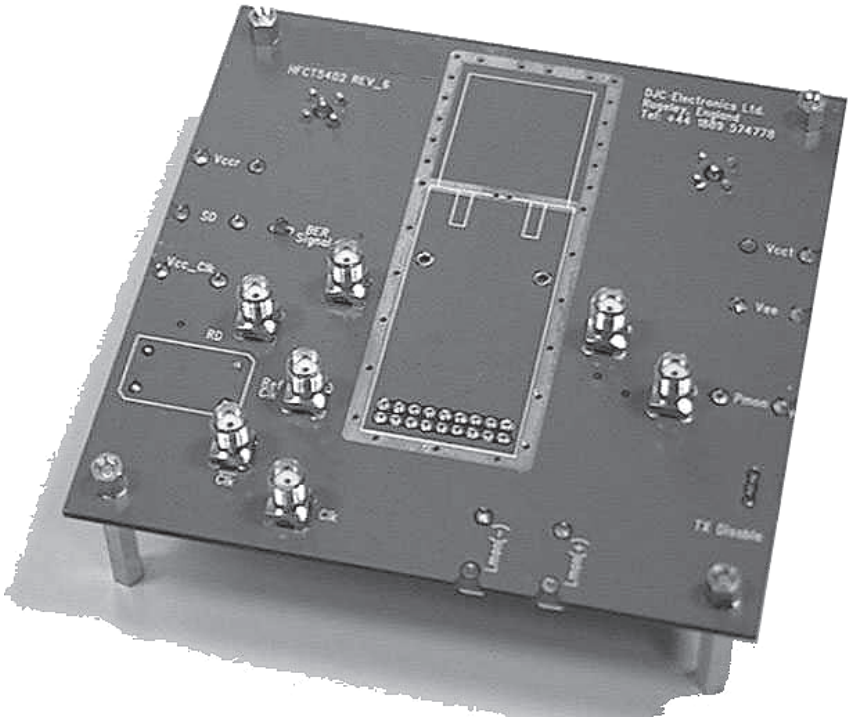


Figure 19. HFCT-5001 Evaluation Board

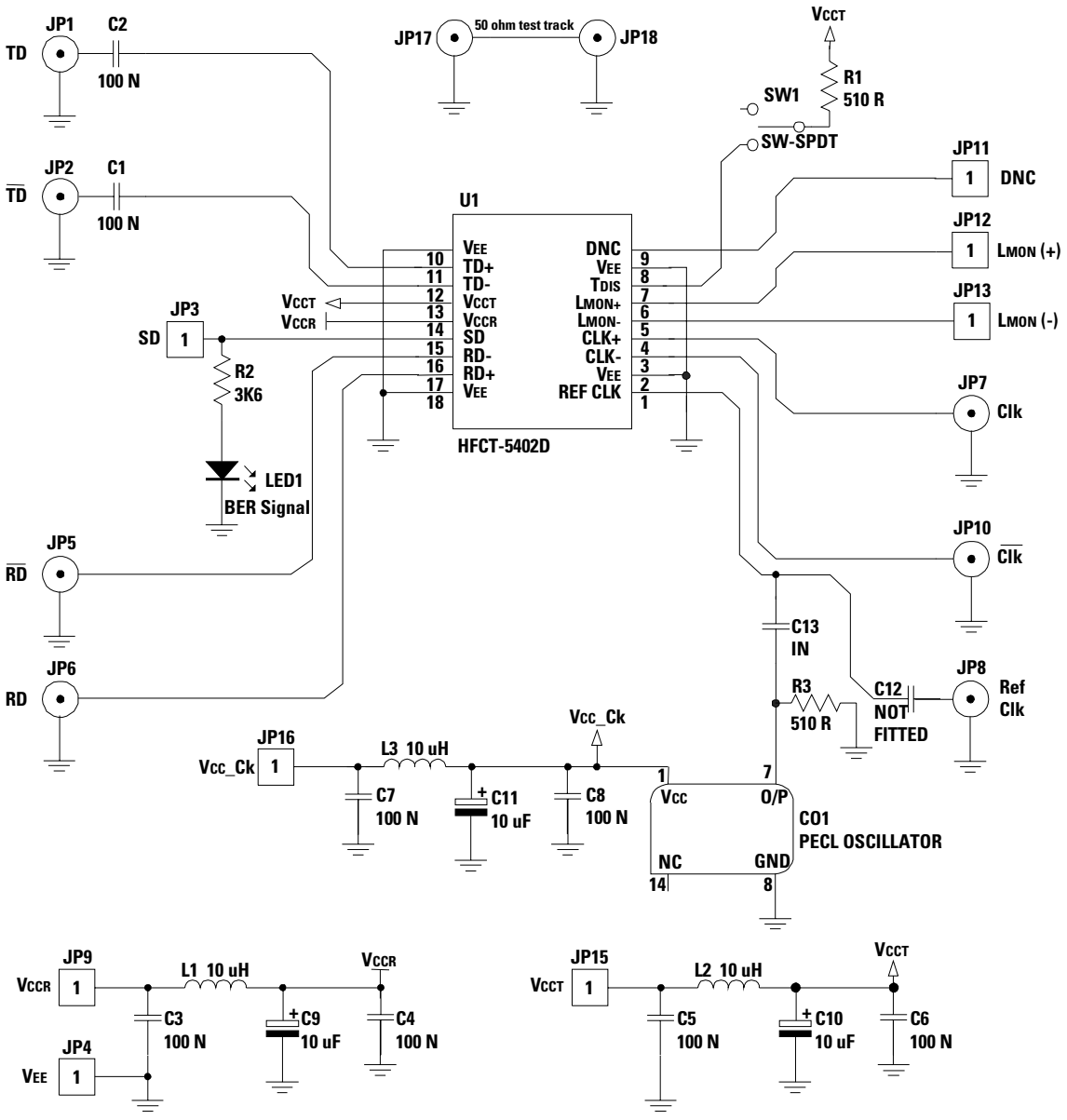


Figure 20. Circuit Schematic for the Evaluation Board

Application Considerations

PCB Layout

Like all RF applications, the PCB design and layout for this high speed transceiver requires careful consideration and attention towards interconnect impedances for DATA and CLOCK nodes. Any form of power supply filtering or decoupling should be done as close as possible to the power supply pins to minimize radiated or conductive pickup.

It is recommended that high speed data and clock tracks be buried striplines to minimize exposure of these lines for EMI suppression. Also, such an approach will ensure signal integrity and avoid waveform degradation from RF interference. Plated through holes or vias used should be as small as possible to avoid impedance discontinuities along interconnecting tracks. Where AC coupling capacitors are required, small 0603 size components are recommended for minimizing variations in track impedances.

EMI Radiation/Susceptibility
EMI suppression becomes increasingly difficult when operating at high data rates. EMI radiation measurements performed to date indicate the need to use external shielding in order to meet FCC Class A chassis emissions requirements. The recommended metal shield for the transceiver is shown in Figure 3. The shield requires good connection to signal ground for effective suppression. The typical emission peaks are at ~2.5 GHz and ~7.5 GHz. It is recommended that the user adopts an approach where the transceiver module is sited within the chassis/rack confines and a short patchcord used to link the transceiver to the optical interface in the front panel.

Front panel mounting is not recommended due to the aperture size required which will not be sufficiently suppressive for frequencies above 7.5 GHz.

Metal bodied simplex/single SC adaptors are recommended for the front panel. This body type is preferred to the all plastic version because it presents a reduced aperture for improved emissions suppression. Duplex SC adaptors are not recommended as the larger aperture required for front panel mounting may allow high frequency radiation.

EMI susceptibility has been tested to 10 V/M field strength with minimal degradation of receiver sensitivity.

Compatibility Trials
The HFCT-5402D transceiver has been evaluated using Vitesse Semiconductors VS8004 and VS8005 Mux/Demux chipsets and compatibility has been confirmed with a 9 dB margin of electrical attenuation between the HFCT-5402D module and the VS8005 Demux inputs. Figure 21 shows the test configuration. An additional Demux is deployed between the pattern generator and the Mux to avoid the need for multiple pattern generators. Also, a 3 dB electrical attenuator is required at the transmitter inputs to prevent the 1.2 V_{p-p} Mux data signal from overloading the Tx inputs of the HFCT-5402D module. Compatibility trials have also been successful using the VSC8062 and VSC8063 chipsets.

A joint reference design combining both the Agilent HFCT-5402D transceiver and AMCC Mux S3041/ Demux S3042 ICs on a common PC board has been completed and good performance achieved. The aim of this exercise was to design a functional board with a view of sharing relevant layout and circuit information with the optics system designer. Figure 22 shows the reference design board. Full description of the design, layout, measurements and results are beyond the scope of this document but a separate document is available. Please contact your Agilent representative for further information.

Recommended Solder and Wash Process
The HFCT-5402D is compatible with industry standard wave or hand solder processes.

HFCT-5402D Process Plug
The HFCT-5402D transceiver is supplied with a process plug for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand +80°C and a rinse pressure of 50 lb/in^2.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals
Solder fluxes used with the HFCT-5402D fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-metals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for the HFCT-5402D are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrolldone.

Regulatory Compliance
The HFCT-5402D is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. Additional information is available from your Agilent sales representative.

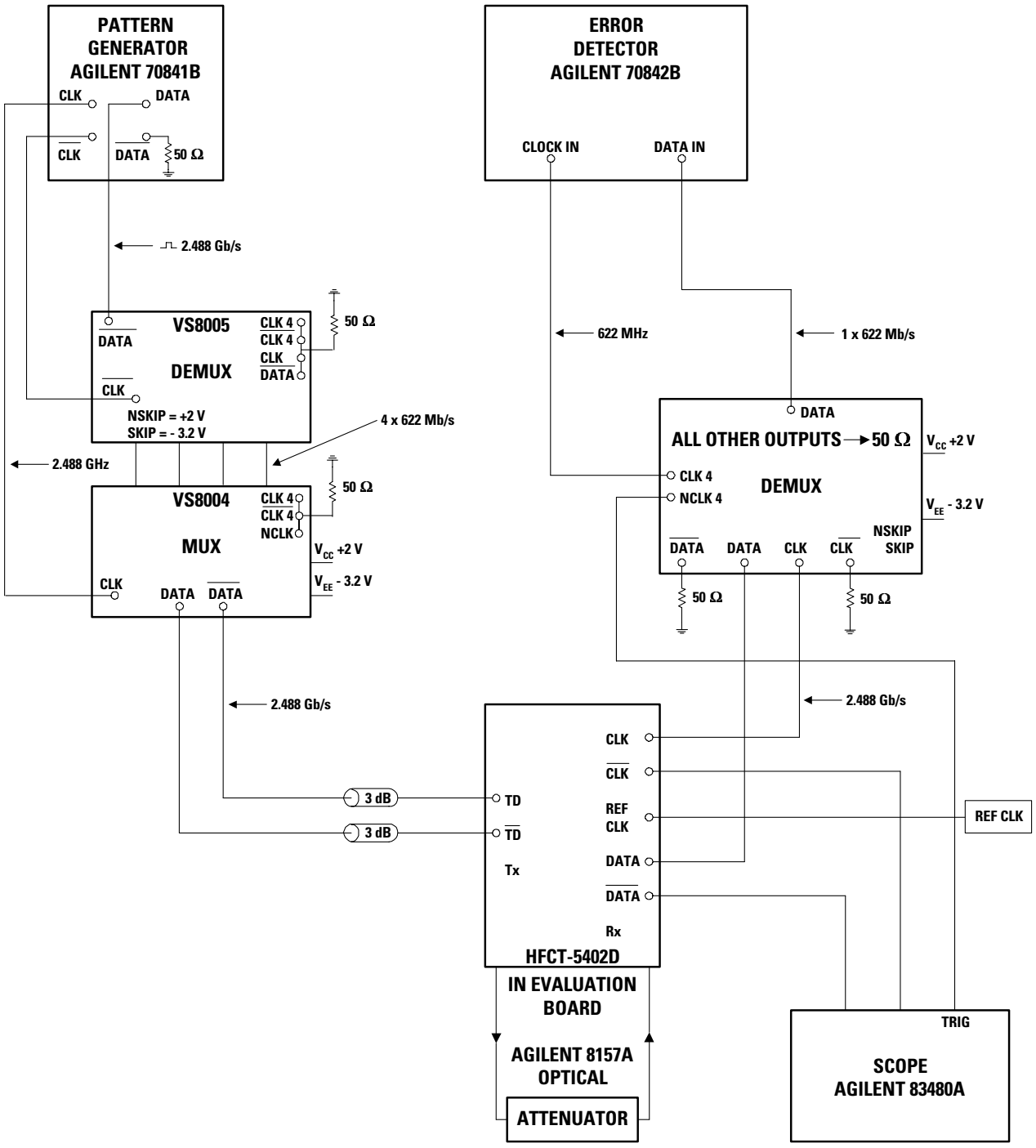


Figure 21. Test Configuration

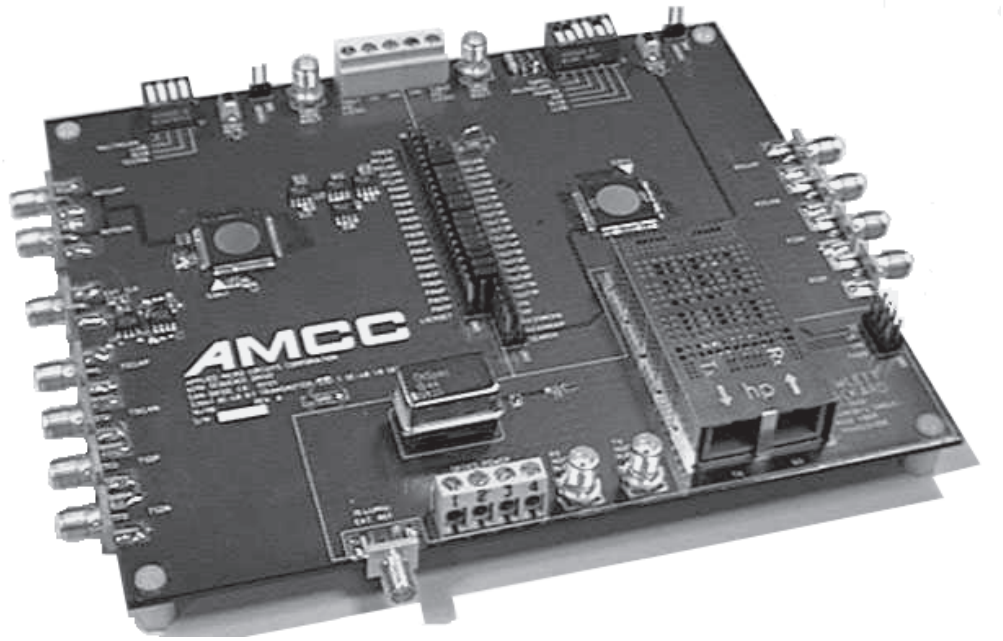


Figure 22. Reference Design Board

Electrostatic Discharge (ESD)

Normal ESD handling precautions for ESD sensitive devices should be followed while using the HFCT-5402D. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas.

Additionally, static discharges to the exterior of the equipment chassis containing the transceiver parts must also be considered. If the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Agilent will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

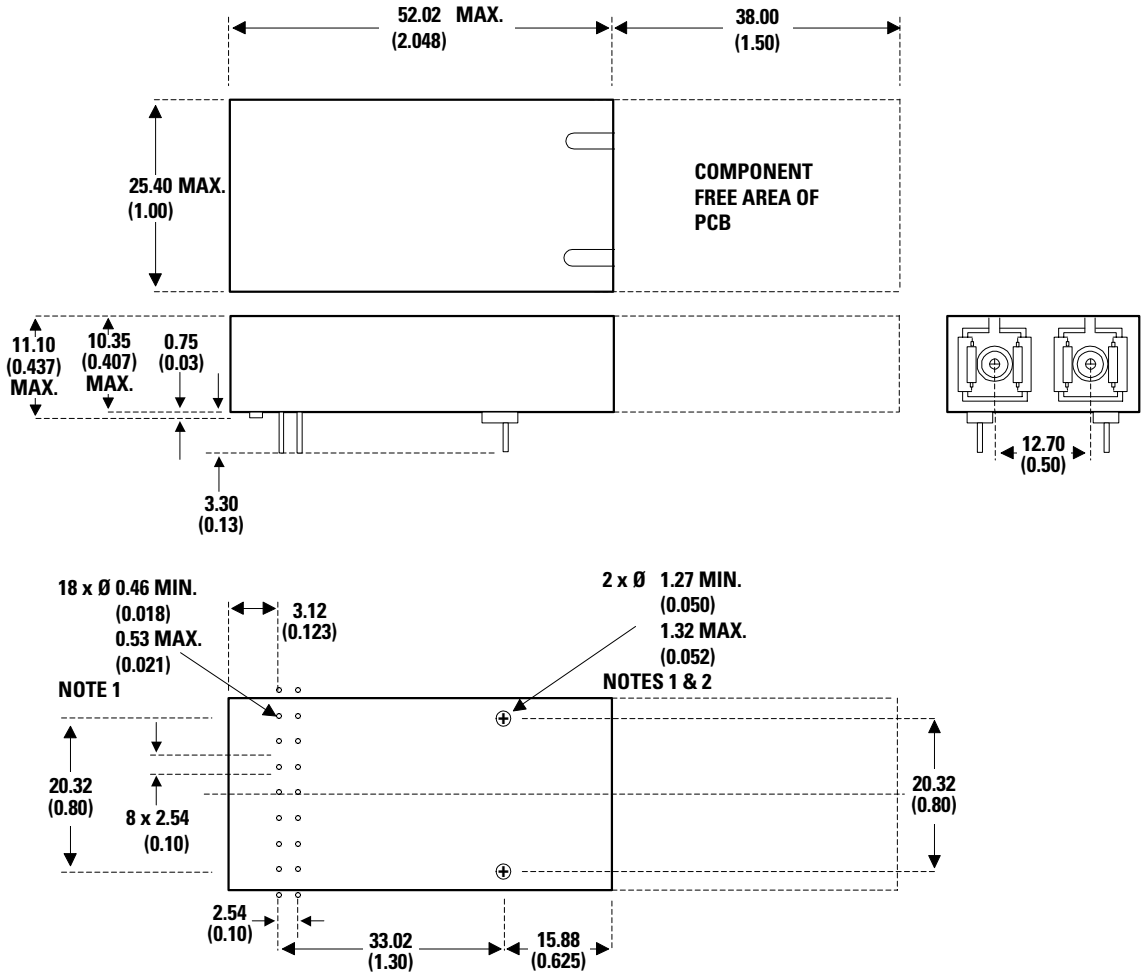
The HFCT-5402D is designed to meet such EMI requirements when used with a recommended shield and positioned inside a well designed chassis. Additionally, an SC duplex jumper cable is recommended for connecting the transceiver to front panel simplex SC optical ports in order to minimize chassis apertures.

Eye Safety

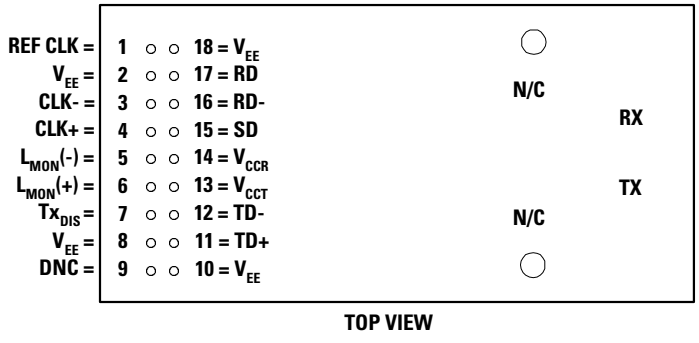
TUV Certification 933/510804 and CDRH Accession 9521220-15 show that the HFCT-5402D is a IEC 825/CDRH Class 1 laser product. Copies available on request.

Qualification

The HFCT-5402D transceivers have been successfully qualified in accordance with the requirements of Bellcore document TA-NWT-000983, under the supervision of Agilent Quality and Reliability Engineering.



NOTES 1: SOLDER POSTS AND ELECTRICAL PINS ARE TIN/LEAD PLATED.
2: SOLDER POSTS ELECTRICALLY ISOLATED TO GROUND.



TOP VIEW

Figure 23. Package Outline Drawing and Pinout

Performance Specifications

Absolute Maximum Ratings[1]

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	+85	°C	-
Lead Soldering Temperature/Time	-	-	+240/10	°C/s	
Input Voltage Swing	V_{IN}	0	2	V	2
Power Supply Voltage	V_{CCT}/V_{CCR}	0	+6	V	
Relative Humidity (Non-Condensing)	RH	0	95	%	

Recommended Operating Environment

Parameter	Symbol	Minimum	Maximum	Units	Notes
Power Supply Voltage	V_{CC}	4.75	5.25	V	-
Ambient Operating Temperature	TA_{OP}	0	+70	°C	3
Airflow		2		m/s	3
Power Supply Noise Tolerance	PSNT		50	mV p-p	4

Transmitter Section

(T_A = 0°C to +70°C, V_{cc} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Center Wavelength	λce	1270	-	1360	nm	-
Output Spectral Width (RMS)	$\Delta\lambda$	-	3	4.0	nm	-
Average Optical Output Power	P_O	-9.5	-5	-3	dBm	5
Extinction Ratio	E_R	8.2	10	-	dB	6
Output Eye	Compliant with Bellcore GR-253-CORE and ITU recommendation G.957					Figure 24
Supply Current	I_{CCT}	-	60	100	mA	7
Power Dissipation	P_{DISS}	-	0.29	0.53	W	
Data Input - Single Ended	V_{IN} p - p	200	-	1100	mV	8 Figure 2b
Data Input - Differential	V_{IN} p - p	400	-	1800	mV	
Transmitter Disable	V_{TXD}	4	-	V_{CCT}	V	
Transmitter Enable	V_{TXE}	V_{EE}	-	3.5	V	

Notes:

1. Not necessarily applied together. Does not guarantee operation under these conditions.
2. Single ended amplitude - see Figure 2 for definition.
3. With recommended metal shield in place and with 2 m/s forced airflow around the transceiver.
4. Between 10 Hz and 10 MHz and using power supply filter circuit as recommended.
5. Output Power is power coupled into a single mode fiber.
6. Measured for TIA/EIA-526-4A.
7. The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum @ maximum temperature (not including termination's) and end of life.
8. Driven into 50 ohm load, measured single-ended.

Receiver Section

(T_A = 0°C to +70°C, V_{cc} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Receiver Sensitivity	-	-	-22	-18.5	dBm	9
Wavelength	-	1270	-	1570	nm	
Maximum Input Power	-	-	-	-3	dBm	9
Supply Current	I_{CCR}	-	200	240	mA	7
Power Dissipation	P_{DISS}	-	1.0	1.3	W	
Data Outputs - Single Ended	-	300	-	-	mV p-p	8
Data Outputs - Differential	-	600	-	-	mV p-p	Figure 2a/b
Clock Outputs - Single Ended	-	250	-	-	mV p-p	8
Clock Outputs - Differential	-	500	-	-	mV p-p	Figure 2a
Clock/Data Alignment	-	50	80	110	ps	10 Figure 2a
Signal Detect Output High	SD_{HIGH}	V_{CCR} -1.3 V	-	V_{CCR}		11
Signal Detect Output Low	SD_{LOW}	V_{EE}	-	V_{EE} +0.8 V		11
Signal Detect Assert	-	-	-	-24	dBm	-
Signal Detect Deassert	-	-45	-	-	dBm	12
Signal Detect Assert Time	-	-	16	-	µs	12
Signal Detect Deassert Time	-	2.3	30	200	µs	13
Ref Clk Input Frequency	-	-	-	19.44 ±100 ppm	MHz	-
Clk Input Rise/Fall$_{TRACE}$	τ_R/τ_F	-	-	7	ns	14 Figure 8
Jitter Tolerance						Figure 13
Jitter Generation	-	-	-	0.01	UI	15
Jitter Transfer	-	-	-	-	-	Figure 14
Reflectance	-	-	-50	-30	dB	16

Notes:

9. Worst case sensitivity and saturation levels for input signals 2^{23}-1 PRBS with 72 ones and 72 zeros inserted with a BER of 10^{-10} (ITU Recommendation G.958), transmitter modulated with an independent data stream.
10. Measured single-ended from clock rising edge to center of data eye.
11. Low Power TTL compatible output introduced to drive ≥10 KΩ load.
12. Complies with Bellcore GR-253-CORE requirements for LOS. SD is $\overline{LOS}$.
13. Over entire dynamic range of receiver.
14. PECL signal input with Figure 8 characteristics.
15. Compliant with Bellcore GR-253-CORE, SONET TI.105.06, SDH G.958.
16. When used with an 8° angled polished SC connector.

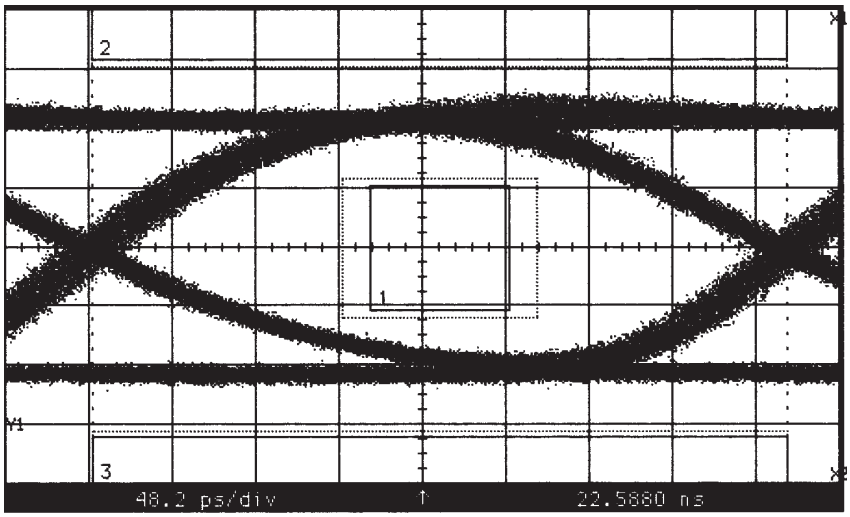


Figure 24. Typical Transmitter Data Eye Diagram with OC-48 Mask

Table 1. HFCT-5402 Transceiver Module Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the nonconductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	Ref Clk	Reference Clock An externally generated clock of 19.44 MHz (For 2.48832 Gb/s) or 1/128 of Bit Rate with a 100 ppm tolerance must be provided for operation of the Clock recovery circuit. This single-ended input requires external ac coupling and clock input of 250 mV p-p minimum, 800 mV p-p maximum and 6 ns maximum rise time. The input stage is internally biased and 50 Ω terminated.
2	V_{EE}	Signal Ground Directly connect this pin to the signal ground plane.
3	Clk-	Received Recovered Clock Out Bar - Internally ac coupled (1 nF). The falling edge occurs in the middle of the Received Data baud period. Terminate this differential clock output with 50 ohms line to the follow-on device. If this output is not used terminate with 50 ohms to V_{EE}.
4	Clk+	Received Recovered Clock Out - Internally ac coupled (1 nF) The rising edge occurs in the middle of the Received Data baud period. Terminate this differential clock output with 50 ohms line to the follow-on device. If this output is not used terminate with 50 ohms to V_{EE}.

Table 1. HFCT-5402 Transceiver Module Pin Out Table (continued)

Pin	Symbol	Functional Description
5	$L_{MON}(-)$	Laser Bias Monitor (-) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
6	$L_{MON}(+)$	Laser Bias Monitor (+) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
7	Tx_{DIS}	Transmitter Disable Transmitter Output Disabled: 4.0 V $\leq$ V7 $\leq$ V_{CCT}. Transmitter Output Enabled: $V_{EET} \leq$ V7 $\leq$ 3.5 V or open circuit.
8	V_{EE}	Signal Ground Directly connect this pin to the signal ground plane.
9	DNC	Do not connect
10	V_{EE}	Signal Ground Directly connect this pin to the signal ground plane.
11	TD+	Transmitter Data In Requires an ac coupled input. The input stage is internally biased and 50 ohm terminated.
12	TD-	Transmitter Data In Bar Requires an ac coupled input. The input stage is internally biased and 50 ohm terminated.
13	V_{CCT}	Transmitter Power Supply Provide +5 V dc via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
14	V_{CCR}	Receiver Power Supply Provide +5 V dc via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
15	SD	Signal Detect Normal input optical data levels above the receiver sensitivity result in a logic “1” output. Loss of optical power to the receiver results in a fault indication shown by a logic “0” output. Signal Detect is a single-ended, internally terminated TTL output. This Signal Detect output can be used to drive a TTL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar input.
16	RD-	Re-timed Receiver Data Out Bar - Internally ac coupled (100 nF) Terminate this differential DATA output with a 50 ohm line and a 50 ohm load at the follow-on device.
17	RD+	Re-timed Receiver Data Out - Internally ac coupled (100 nF) Terminate this differential DATA output with a 50 ohm line and a 50 ohm load at the follow-on device.
18	V_{EE}	Signal Ground Directly connect this pin to signal ground plane.

Ordering Information

HFCT-5402D - 2.5 Gb/s with EMC Diffuser Shield

Associated Parts

HFCT-5001 - HFCT-5402 Evaluation Board

HFCT-5400 - EMC Diffuser Shield

Class 1 Laser Product: This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture
Date of Manufacture: _____
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